

# 2002 VFD Display Module User's Guide

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## NOTES:

Product Version : Ver 1.0

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## **Chapter 1. Overview**

## 1.1 Overview

Thanks for using this 20\*2 display module which is a compact and light-weight unit by using new VFD (Vacuum Fluorescent Display) technology. This product can provide excellent visual recognition by means of a clear display with high brightness, less eye fatigue compared to LED (soft light), wide viewing angle, operating at low voltage with low power consumption.

## 1.2 Features

- Simple connection to the host system data bus via three-wired synchronous serial interface (/STB, SCK, SIO)
- Since a DC-DC/AC converter is used, only +5VDC power source is required to operate the module
- · High quality of display and luminance
- Compact and light-weight unit by using new VFD technology and flat packed one-chip controller
- Luminance adjustment available by software (4 levels)
- 8 user definable fonts available (CG-RAM font)
- ASCII and Japanese characters (CG-ROM font)

## Chapter 2. Hardware Detail

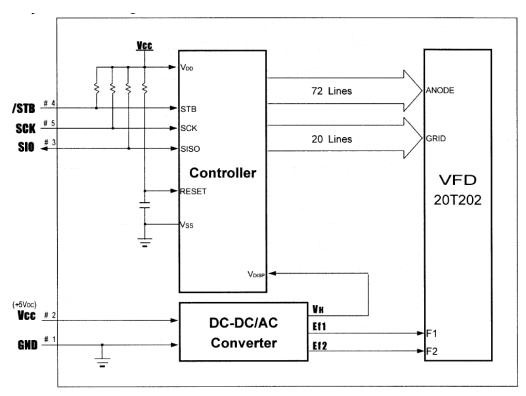
## 2.1 Pin Definition

**TABLE 2-1 PIN DEFINITION** 

No.	Pin	Description
1	GND	Ground
2	V <sub>CC</sub>	Power supply (+5V <sub>DC</sub> is required.)
3	SIO	Input/output terminal for display or control codes
4	/STB	Strobe input
5	SCK	Shift clock input terminal of shift register

## 2.2 System Block Diagram

## FIGURE 2-1 SYSTEM BLOCK DIAGRAM OF THIS VFD MODULE



## **Chapter 3. Electrical Characteristics**

## 3.1 Environment Condition

### **TABLE 3-1 ENVIRONMENT CONDITION**

Parameter	Symbol	Min.	Тур.	Max.	Unit
Operating Temperature	$T_{opr}$	-20	+25	+70	$^{\circ}$
Storage Temperature	$T_{stg}$	-40	-	+85	$^{\circ}$
Humidity (Operating)	$H_{opr}$	0	-	85	%
Humidity (Non-operating)	$H_{\text{stg}}$	0	-	90	%
Vibration (10 – 55Hz)	-	-	-	4	G
Shock	-	-	-	40	G

## 3.2 Absolute Maximum Ratings

## **TABLE 3-2 ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	V <sub>CC</sub>	-0.5	6.0	$V_{DC}$
Input Signal Voltage	V <sub>IS</sub>	-0.5	V <sub>CC</sub> + 0.5	$V_{DC}$

## 3.3 Recommended Operating Conditions

## **TABLE 3-3 RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Min.	Тур.	Max.	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	$V_{DC}$
Signal (Logic) Input Voltage	V <sub>IS</sub>	0	-	$V_{CC}$	$V_{DC}$
Operating Temperature	T <sub>OPR</sub>	-20	+25	+70	$^{\circ}$

## 3.4 DC Characteristics

## TABLE 3-4 DC CHARACTERISTICS ( $T_a = +25^{\circ}C$ , $V_{CC} = +5.0 V_{DC}$ )

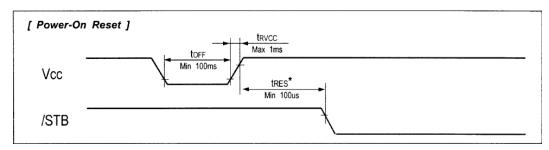
Parameter		Symbol	Min.	Тур.	Max.	Unit
Supply Current '	*	I <sub>CC</sub>	-	150	220	mA
Logic Input	"H" Level	V <sub>IH</sub>	0.8×V <sub>CC</sub>	-	-	$V_{DC}$
Voltage	"L" Level	$V_{IL}$	-	-	0.2×V <sub>CC</sub>	$V_{DC}$
"H" Level Input Current	V <sub>IN</sub> =V <sub>CC</sub>	I <sub>IH</sub>	20	-	500	uA
Luminance		L	100 (340)	200 (680)	-	ft-L (cd/m <sup>2</sup> )

**Note:** \* I<sub>CC</sub> shows the current when all dots are turned on. The surge current can be approx. 3 times the specified supply current at power on. However, the exact peak surge current amplitude and duration are dependent on the characteristics of the host power supply.

## 3.5 Timing Chart and AC Characteristics

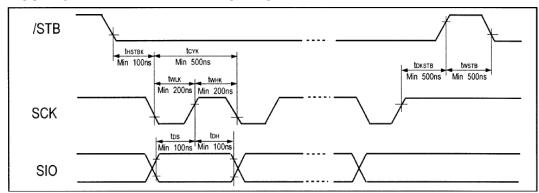
## 3.5.1 RESET Timing

## FIGURE 3-1 POWER-ON RESET AND RESET SIGNAL TIMING



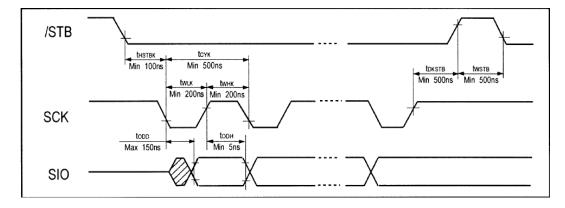
## 3.5.2 Serial Input (Write) Timing

## FIGURE 3-2 DATA WRITE-IN TIMING DIAGRAM



## 3.5.3 Serial Output (Read) Timing

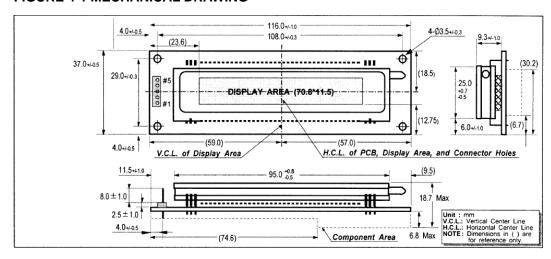
## FIGURE 3-3 DATA READ-OUT TIMING DIAGRAM



## **Chapter 4. Mechanical Drawing**

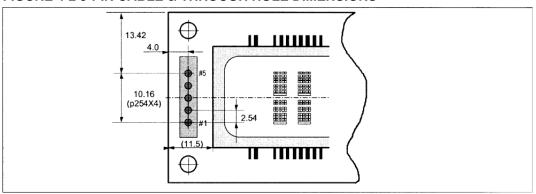
## 4.1 Mechanical Drawing

### FIGURE 4-1 MECHANICAL DRAWING



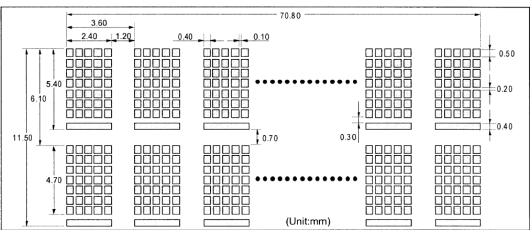
## 4.2 Connector Cable Location

## FIGURE 4-2 5-PIN CABLE & THROUGH HOLE DIMENSIONS



### 4.3 Pattern Details

### **FIGURE 4-3 PATTERN DETAILS**





## Chapter 5. Appendix

## 5.1 Function Descriptions

## 5.1.1 Registers in VFD Controller

The VFD controller has two 8-bit registers, an instruction register (IR) and a data register (DR). IR stores instruction codes, such as display clear and cursor shift, and address information for DD-RAM and CG-RAM. The IR can only be written from the host MPU. DR temporarily stores data to be written into DD-RAM or CG-RAM and temporarily stores data to be read from DD-RAM or CG-RAM. Data written into the DR from the MPU is automatically written into DD-RAM or CG-RAM by an internal operation. The DR is also used for data storage when reading data from DD-RAM or CG-RAM. When address information is written into the IR, data is read and then stored into the DR from DD-RAM or CG-RAM by internal operation. Data transfer between MPU is then completed when the MPU reads the DR. After the read, data in DD-RAM or CG-RAM at the next address is sent to the DR for the next read from the MPU. By the register selector (RS) signal, these two registers can be selected.

### **TABLE 5-1 REGISTER SELECTION**

RS	R/W	Description
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB7) and address counter (DB0 to DB6)
1	0	DR write as an internal operation (DR to DDRAM or CGRAM)
1	1	DR read as an internal operation (DDRAM or CGRAM to DR)

### 5.1.1.1 Address Counter (ACC)

The address counter (ACC) assigns addresses to both DD-RAM and CG-RAM. When an address of an instruction is written into the IR, the address information is sent form the IR to the ACC. Selection of either DD-RAM or CG-RAM is also determined concurrently by the instruction. After writing into (reading from) DD-RAM or CG-RAM, the ACC is automatically incremented by 1 (decremented by 1). The ACC contents are then output to DB0 to DB6 when RS=0 and R/W=1. (See table 5-1)

### 5.1.1.2 Display Data RAM (DD-RAM)

Display data RAM (DD-RAM) stores display data represented in 8-bit character codes. The area in DD-RAM that is not used for display can be used as general data RAM. See table 5-2 for the relationships between DD-RAM addresses and positions on the VFD.

TABLE 5-2 RELATION BETWEEN DIGIT POSITION AND DD-RAM DATA

	Left End	2nd Column	3rd Column	 19th Column	Right End
1st Row	00 Hex	01 Hex	02 Hex	 12 Hex	13 Hex
2nd Row	40 Hex	41 Hex	42 Hex	 52 Hex	53 Hex

## 5.1.1.3 Character Generator ROM (CG-ROM)

The CG-ROM generates character patterns of 5x7 dots from 8-bit character codes (figure 5-2). It can generate 240 kinds of 5x7 dot character patterns. The character fonts are shown on the following page. The character codes 00H to 0FH are allocated to the

CG-RAM.

## 5.1.1.4 Character Generator RAM (CG-RAM)

In the character generator RAM (CG-RAM), the user can rewrite character patterns by program. For 5x7 dots and cursor, eight patterns can be written. Write into DD-RAM the character codes at the addresses shown as the left column of figure 5-2 to show the character patterns stored in CG-RAM. See figure 5-3 for the relationship between CG-RAM addresses and data and display patterns and refer to figure 5-1 for dot assignment of VFD. Areas that are not used for display can be used as general data RAM.

## **FIGURE 5-1 DOT ASSIGNMENT**

1	2	3	4	5
6	7	8	9	10
11	12	13	14	15
16	17	18	19	20
21	22	23	24	25
26	27	28	29	30
31	32	33	34	35
		36		

## FIGURE 5-2 CHARACTERS FONT (CG-ROM) AND CG-RAM CODES

	Up	per	bits	DB7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
				DB6	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
Lo	ver	bits		DB5 DB4	0	0	0	1	0	0	0	1	0	0 1	0	1	0	0	0	1
				DD4				-					_			i i	_	-		
DB3	DB2	DB1	DB0		0	1	2	3	4	5	6	7	8	9	Α	В	С	D	E	F
0	0	0	0	0	CG-RAM (1)									E			7			
0	0	0	1	1	CG-RAM (2)									#						
0	0	1	0	2	CG-RAM (3)					R										
0	0	1	1	3	CG-RAM] (4)		Ħ													
0	1	0	0	4	CG-RAM (5)												k			
0	1	0	1	5	CG-RAM (6)			5								Ħ				
0	1	1	0	6	CG-RAM (7)		8	8	F							Ħ				
0	1	1	1	7	CG-RAM (8)												×			П
1	0	0	0	8	CG-RAM (1)			8		×	h		ø							<b>*</b>
1	0	0	1	9	CG-RAM (2)	H				¥						T				
1	0	1	0	A	CG-RAM (3)					2				ď				Þ	j	
1	0	1	1	В	CG-RAM] (4)			<b>P</b>	K		×		ű							Ħ
1	1	0	0	С	CG-RAM (5)					Ħ	1								4	H
1	1	0	1	D	CG-RAM (6)				H		m		#						Ł	
1	1	1	0	Е	CG-RAM (7)				H		m								Ħ	
1	1	1	1	F	CG-RAM (8)						o								6	Carried Control of the Control of th

# FIGURE 5-3 RELATIONSHIP BETWEEN CG-RAM ADDRESSES, CHARACTER CODES (DD-RAM) AND 5X7 (WITH CURSOR) DOT CHARACTER PATTERNS (CG-RAM DATA)

						ode				co	G-R	AM	Ad	dre	ss			(		racte					
E 7		D B 6	D B 5	D B 4	D B 3	D B 2	D B 1	D B 0		<b>A</b> 5	A4	А3	A2	A1	A0		D B 7	D B 6	D B 5	D B 4	D B 3	D B 2	D B 1	D B 0	
Γ	T												0	0	0		х	х	х	1	2	3	4	5	
													0	0	1		x	x	x	6	7	8	9	10	
													0	1	0		х	x	x	11	12	13	14	15	
1		0	0	0	x	0	0	0		0	0	0	0	1	1		x	x	x	16	17	18	19	20	Character Pattern(1)
1,	' '	١	٦	U	*	Ů	٥	١		١	١	U	1	0	0		x	x	x	21	22	23	24	25	
													1	0	1		х	x	x	26	27	28	29	30	
													1	1	0		x	x	x	31	32	33	34	35	Cursor
L	$\perp$								L				1	1	1		х	x	x	36	x	x	x	x	position
													0	0	0		x	x	x	1	2	3	4	5	\ '
													0	0	1		x	x	X	6	7	8	9	10	
													0	1	0		х	x	X	11	12	13	14	15	Character
1		0	0	0	x	0	0	1		0	0	1	0	1	1		x	x	x	16	17	18	19	20	Character Pattern(2)
													1	0	0		х	x	x	21	22	23	24	25	
													1	0	1		х	X	X	26	27	28	29	30	
													1	1	0		x	X	X	31	32	33	34	35	Cursor
$\vdash$	+	4							<u> </u>	_		_	1	1	1	_	х	х	X	36	X	X	X	х	position
													0	0	0		х	X	X	1	2	3	4	5	
Ι.													0	0	1		X	х	X	6	7	8	9	10	
1	' '	0	0	0	X	0	1	0		0	1	0	0	1	0		х	X	X	11	12	13	14	15	
		ليـ	_	_	_	$\vdash$	_	_	-		_		0	1	1		x	X	X	16	17	18	19		! !
T	T.		_											-		$\vdash$	_	_	<u></u>	200	27	20	20	20	
1	"	0	0	0	x	1	1	1		1	1	1	1	0	1		X	X	X	26 31	27 32	33	29 34	30 35	
													1	1	1		x	x	X	36	32 X	33 X	34 X	-	
L						<u> </u>	L	L	L	<u> </u>	L	L	<u> </u>		<u>'</u>	L_		X		36	X	<u> </u>	X	х	1

## Note:

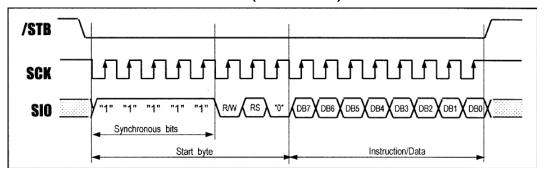
- 1. Character code bits 0 to 2 correspond to CG-RAM address bits 3 to 5 (3 bits: 8 types).
- 2. CG-RAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor. Maintain the 8th line data, corresponding to the cursor display position, at 0 as the cursor display. If bit 4 of the 8th line data is 1, 1 bit will light up the cursor regardless of the cursor presence.
- 3. Character pattern row positions correspond to CG-RAM data bits 0 to 4 (bit 4 being at the left).
- 4. As shown in figure 5-3, CG-RAM character patterns are selected when character code bits 4 to 7 are all 0. However, since character code bit 3 has no effect, the R display example above can be selected by either character code 00H or 08H.
- 5. 1 for CG-RAM data corresponds to display selection and 0 to non-selection.
- 6. "x" indicates no effect.

## 5.1.2 Data Transfer

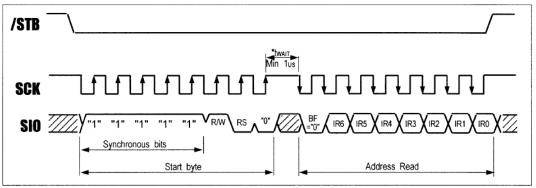
When data written, data can be input when strobe goes "0". 1st byte is Start byte, register to select IR or DR by RS (bit 6) bit and data write or read by R/W (bit 5=0) in this byte. And next byte is instruction byte. (See figure 5-4)

When data is read, to read the Busy flag + Address counter (AC6 to AC0) or to read the data which was written in DD-RAM or CG-RAM is chosen by the start byte to input first. Data is output at the falling edge of the shift clock (See figure 5-5 and figure 5-6).

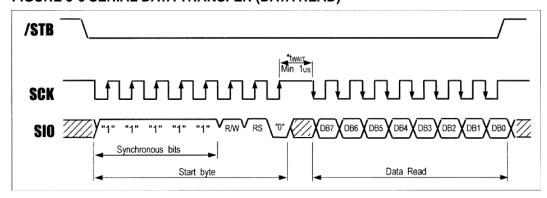
## FIGURE 5-4 SERIAL DATA TRANSFER (DATA WRITE)



## FIGURE 5-5 SERIAL DATA TRANSFER (ADDRESS READ)



## FIGURE 5-6 SERIAL DATA TRANSFER (DATA READ)



**Note:** t<sub>WAIT</sub>: wait time

## 5.1.3 Reset Function

An internal reset circuit automatically initializes the module when the power is turned on. The following instructions are executed during the initialization.

1. Display clear

Fill the DD-RAM with 20H (Space Code).

2. Set the address counter to 00H

Set the address counter (ACC) to point DD-RAM.

3. Display on/off control:

D=0 ; Display off C=0 ; Cursor off B=0 ; Blinking off

4. Entry mode set:

I/D=1 ; Increment by 1

S=0 ; No shift

5. Function set

N=1 ; 2-line display BR0=BR1=0 ; Brightness=100%

## 5.2 Instruction

### 5.2.1 Outline

Only the instruction register (IR) and the data register (DR) of the VFD controller can be controlled by the user's MPU. Before starting the internal operation of the controller, control information is temporarily stored into these registers to allow interfacing with various MPUs, which operate at different speeds, or various peripheral control devices. The internal operation of the controller is determined by signals sent from the MPU. These signals, which include register selection signal (RS), read/write (R/W), and the data bus (DB0 to DB7), make up the controller instructions (see figure 5-7). There are four categories of instructions that:

- Designate controller functions, such as display format, data length, etc.
- Set internal RAM addresses
- Perform data transfer with internal RAM
- · Perform miscellaneous functions

Normally, instructions that perform data transfer with internal RAM are used the most. However, auto-increment by 1 (or auto-decrement by 1) of internal RAM addresses after each data write can lighten the program load of the MPU. Since the display shift instruction can perform concurrently with display data write, the user can minimize system development time with maximum programming efficiency.

## FIGURE 5-7 SINSTRUCTION SET

Instruction CODE											
instruction	RS   R/W   DB7   DB6   DB5   DB4   DB3   DB2   DB1   DB0										
Display Clear							1	Clears all display and sets DD-RAM address 0 in address counter.			
Cursor Home	0	0	0	0	0	0	0	0	1	x	Sets DDRAM address 0 in ACC. Also returns the display being shifted to the original position. DD- RAM contents remain unchanged.
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	s	Sets the cursor direction and specifies display shift. These operations are performed during writing/reading data.
Display ON/OFF Control	0	0	0	0	0	0	1	D	С	В	Sets all display ON/OFF(D), cursor ON/OFF(C), cursor blink of character position(B)
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	x	x	Shifts display or cursor, keeping DD-RAM contents.
Function Set	unction Set 0 0 0 0 1 IF N x BR1 BR0 di							Sets data length(IF), number of display lines(N), Set brightness level(BR1,BR0)			
CGRAM Address Setting	0	0	0	1			AC	G			Sets the CG-RAM address.
DDRAM Address Setting	0	0	1				ADD			***************************************	Sets the DD-RAM address.
Busy Flag & Address Reading	0	o i Br Acc counter								Read busy flag(BF) and address counter (ACC).	
Data Writing to CG or DDRAM	1	0				Data	Writes data into CG-RAM or DDRAM.				
Data Reading from CG or DDRAM	1 1 Data reading										Reads data from CG-RAM or DDRAM.
		1 : Ir 0 : D				[ Abbreviation ]					
	S =	: 1 : I : 0 : (	Cursoi	shift	enab		DD-RAM: Display Data RAM  CG-RAM: Character Generator  RAM				
	S/C =	0 : 0	Curso	mov	е		ACG : CG-RAM Address				
		1:5					ADD : DD-RAM Address				
		1 : 8 0 : 4									ACC : Address Counter
		: 1 : 2 : 0 :									
	BR1,	BR0	01 10	: 100° : 75° : 50° : 25°	% %						
		• 1 : I • 0 : I						able)			
	x : D	on't C	are								

## **5.2.2 Instruction Description**

## 5.2.2.1 Display Clear

## FIGURE 5-8 DISPLAY CLEAR INSTRUCTION

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	0	0	1	01H
RS = 0	P/W	= 0						1

## This instruction:

- Fills all locations in the display data RAM (DD-RAM) with 20H (Blank-character).
- Clears the contents of the address counter (ACC) to 00H.
- Sets the display for zero character shift (returns original position).

- Sets the address counter (ACC) to point to the DD-RAM.
- If the cursor is displayed, moves the cursor to the left most character in the top line (upper line).
- Sets the address counter (ACC) to increment on the each access of DD-RAM or CG-RAM.

### 5.2.2.2 Cursor Home

### FIGURE 5-9 CURSOR HOME INSTRUCTION

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	0	1	х	02H to 03H
RS = (	), R/W	= 0						x : Don't care

### This instruction:

- Clears the contents of the address counter (ACC) to 00H.
- Sets the address counter (ACC) to point to the DD-RAM.
- Sets the display for zero character shift (returns original position).
- If the cursor is displayed, moves the left most character in the top line (upper line).

## 5.2.2.3 Entry Mode Set

## **FIGURE 5-10 INSTRUCTION**

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	_
0	0	0	0	0	1	I/D	S	04H to 07H
RS = (	). R/W	= 0						

The I/D bit selects the way in which the contents of the address counter (ACC) are modified after every access to DD-RAM or CG-RAM.

I/D=1: The address counter (ACC) is increased.

I/D=0: The address counter (ACC) is decreased.

The S bit enables display shift, instead of cursor shift, after each write or read to the DD-RAM.

S=1: Display shift enabled.

S=0: Cursor shift enabled.

The direction in which the display is shifted is opposite in sense to that of the cursor. For example, if S=0 and I/D=1, the cursor would shift one character to the right after a MPU writes to DD-RAM. However if S=1 and I/D=1, the display would shift one character to the left and the cursor would maintain its position on the panel.

The cursor will already be shifted in the direction selected by I/D during reads of the DD-RAM, irrespective of the value of S. similarly reading and writing the CG-RAM always shift the cursor. Also both lines are shifted simultaneously.

TABLE 5-3 CURSOR MOVE AND DISPLAY SHIFT BY THE "ENTRY MODE SET"

I/D	S	After writing DD-RAM data	After reading DD-RAM data
		The cursor moves one character to	The cursor moves one character to
0	0	the left.	the left.
1	0	The cursor moves one character to	The cursor moves one character to
'		the right.	the right.
	4	The display shifts one character to	The cursor moves one character to
U	I	the right without cursor's move.	the left.

1	1	The display shifts one character to	The cursor moves one character to
ı	'	the left without cursor's move	the right

## 5.2.2.4 Display ON/OFF

### FIGURE 5-11 DISPLAY ON/OFF INSTRUCTION

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	1	D	С	В	08H to 0FH

RS = 0, R/W = 0

This instruction controls various features of the display.

D=1: Display on, D=0: Display off C=1: Cursor on, C=0: Cursor off B=1: Blinking on, B=0: Blinking off

**Note:** Blinking is achieved by alternating between a normal and all on display of a character. The cursor blinks with a frequency of about 1.0 Hz and DUTY 50%.

## 5.2.2.5 Cursor/Display Shift

#### FIGURE 5-12 CURSOR/DISPLAY SHIFT INSTRUCTION

						DB1		
0	0	0	1	S/C	R/L	х	x	10H to 1FH (x: Don't care)
RS = (	), R/W	= 0						_

This instruction shifts the display and/or moves the cursor, one character to the left or right, without reading or writing DD-RAM.

The S/C bit selects movement of the cursor or movement of both the cursor and the display.

S/C=1: Shift both cursor and display

S/C=0: Shift cursor only

The R/L bit selects left ward or right ward movement of the display and/or cursor.

R/L=1: Shift one character right

R/L=0: Shift one character left

## **TABLE 5-4 CURSOR/DISPLAY SHIFT**

S/C	R/L	Cursor Shift	Display Shift
0	0	Move one character to the left	Do Shift
0	1	Move one character to the right	Do Shift
1	0	Shift one character to the left with display	Shift one character to the left
1	1	Shift one character to the right with display	Shift one character to the right

## 5.2.2.6 Function Set

## FIGURE 5-13 FUNCTION SET INSTRUCTION

	DB6							
0	0	1	1	N	х	BR1	BR0	20H to 3FH
RS = (	x : Don't care							

This instruction sets the number of display line and brightness control. This instruction initializes the system, and must be the first instruction executed after power-on.

The N bit selects between 1-line or 2-line display.

N=1: Select 2 line display (Using anode output A1 to A80)

N=0: Select 1 line display (Using anode output A1 to A40. A41 to A80 fixed Low

level.)

BR1, BR0 flag is control to brightness of VFD to modulate pulse width of anode output as follows.

## FIGURE 5-14 BR1, BR0 FLAG AND BRIGHTNESS

BR1	BR0	Brightness
~~~	~~~	~~~~~~
0	0	100 %
0	1	75 %
1	0	50 %
1	1	25 %

### 5.2.2.7 Set CG-RAM Address

#### FIGURE 5-15 SET CG-RAM ADDRESS

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	1			A	CG			40H to 7FH
RS = (	), R/W	= 0						

### This instruction:

- Load a new 6-bit address into the address counter (ACC).
- Sets the address counter (ACC) to address CG-RAM.

Once "Set CG-RAM Address" has been executed, the contents of the address counter (ACC) will be automatically modified after every access of CG-RAM, as determined by the "Entry Mode Set" instruction. The active width of the address counter (ACC), when it is addressing CG-RAM, is 6 bits, so the counter will wrap around to 00H from 3FH if more than 64 bytes of data are written to CG-RAM.

## 5.2.2.8 Set DD-RAM Address

## FIGURE 5-16 SET DD-RAM ADDRESS

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
1				ADD				80H to A7H (1-Line)
RS =	0, R/	W = 0						C0H to E7H (2-Line)

### This instruction:

- Load a new 7-bit address into the address counter (ACC).
- Sets the address counter (ACC) to point to the DD-RAM.

Once "Set DD-RAM Address" instruction has been executed, the contents of the address counter (ACC) will be automatically modified after each access of DD-RAM, as selected by the "Entry Mode Set" instruction.

## **TABLE 5-5 VALID DD-RAM ADDRESS RANGES**

	Number of Character	Address Range		
1st line	40	00H to 27H		
2nd line	40	40H to 67H		

5.2.2.9 Read Address

#### **FIGURE 5-17 READ ADDRESS**

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
BF=0				ACC			

RS = 0, R/W = 1

The next instruction will not be accepted until BF is reset to 0. Check the BF status before the next write operation. At the same time, the value of the address counter (ACC) in binary AAAAAAA is read out. This address counter (ACC) is used by both CG-RAM and DD-RAM addresses, and its value is determined by the previous instruction. The address contents are the same as for instructions set CG-RAM address and set DD-RAM address.

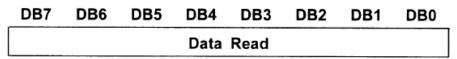
## 5.2.2.10Write Data to CG or DD-RAM

FIGURE 5-18 WRITE DATA TO CG OR DD-RAM

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
	00H to	FFH							
RS =	1, R/W	= 0							

This instruction writes 8-bit binary data (DB7 to DB0) into CG-RAM or DD-RAM. To write into CG-RAM or DD-RAM is determined by the previous specification of the CG-RAM or DD-RAM address setting. After a write, the address is automatically incremented or decremented by 1 according to the entry mode. The entry mode also determines the display shift. When data is written to the CG-RAM, the DB7, DB6 and Db5 bits are not displayed as characters.

# 5.2.2.11 Read Data from CG or DD-RAM FIGURE 5-19 READ DATA TO CG OR DD-RAM



RS = 1, R/W = 1

This instruction reads 8-bits binary data (DB7 to DB0) from CG-RAN or DD-RAM. The previous designation determines whether CG-RAM or DD-RAM is to be read. Before entering this read instruction, either CG-RAM or DD-RAM address set instruction must be executed. If not executed, the first read data will be invalid. When serially executing read instructions, the next address data is normally read from the second read. The address set instructions need not be executed just before this read instruction when shifting the cursor by the cursor shift instruction (when reading out DD-RAM). The operation of the cursor shift instruction is the same as the set DD-RAM address instruction. After a read, the entry mode automatically increases or decreases the address by 1.

**Note:** The address counter (ACC) is automatically increased or decreased by 1 after the write instructions to CG-RAM or DD-RAM are executed. The RAM data selected by the ACC cannot be read out at this time even if read instructions are executed. Therefore, to correctly read data, execute either the address set instruction or cursor shift instruction (only with DD-RAM), then just before reading the desired data, execute the read instruction from the second time the read instruction is sent.

## 5.3 Operating Recommendations

- Avoid applying excessive shock or vibration beyond the specification for the VFD module.
- Since VFDs are made of glass material, careful handling is required. i.e. Direct impact with hard material to the glass surface (especially exhaust tip) may crack the glass.
- When mounting the VFD module to your system, leave a slight gap between the VFD glass and your front panel. The module should be mounted without stress to avoid flexing of the PCB.
- Avoid plugging or unplugging the interface connection with the power on, otherwise it may cause the severe damage to input circuitry.
- Exceeding any of maximum ratings may cause the permanent damage.
- Since the VFD modules contain high voltage source, careful handling is required during powered on.
- When the power is turned off, the capacitor does not discharge immediately. The high voltage applied to the VFD must not contact to the ICs. And short-circuit of mounted components on PCB within 30 seconds after power-off may cause damage to those.
- The power supply must be capable of providing at least 3 times the rated current, because the surge current can be more than 3 times the specified current consumption when the power is turned on.
- Avoid using the module where excessive noise interference is expected. Noise may
  affects the interface signal and causes improper operation. And it is important to
  keep the length of the interface cable less than 50cm.
- Since all VFD modules contain C-MOS ICs, anti-static handling procedures are always required.



## Chapter 6. Contact Us

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